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Terms	Documents
hardware\$ near4 accelerat\$ and (central processor or cpu) and (byte code)and stack\$ and register\$ and (conver\$ or translat\$) near9 (stack\$ near4 register\$)	0

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<u>L11</u>	hardware\$ near4 accelerat\$ and (central processor or cpu) and (byte code)and stack\$ and register\$ and (conver\$ or translat\$) near9 (stack\$ near4 register\$)	0	<u>L11</u>
	<i>DB=DWPI; PLUR=YES; OP=ADJ</i>		
<u>L10</u>	hardware\$ near4 accelerat\$ and (central processor or cpu) and (byte code)and stack\$ and register\$ and (conver\$ or translat\$) near9 (stack\$ near4 register\$)	0	<u>L10</u>
	<i>DB=JPAB; PLUR=YES; OP=ADJ</i>		
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<u>L7</u>	hardware\$ near4 accelerat\$ and (central processor or cpu) and (byte code)and stack\$ and register\$ and (conver\$ or translat\$) near9 (stack\$ near4 register\$) <i>DB=PGPB; PLUR=YES; OP=ADJ.</i>	0	<u>L7</u>
<u>L6</u>	hardware\$ near4 accelerat\$ and (central processor or cpu) and (byte code)and stack\$ and register\$ and (conver\$ or translat\$) near9 (stack\$ near4 register\$) <i>DB=USPT; PLUR=YES; OP=ADJ.</i>	4	<u>L6</u>
<u>L5</u>	L4 and l2	3	<u>L5</u>
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<u>L2</u>	L1 and stack\$ and register\$	20	<u>L2</u>
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Terms used

[hardware accelerator](#) and [cpu](#) and [java](#) and [byte code](#) and [reigester](#) and [stack](#)

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**1 Improving Java performance using hardware translation**

Ramesh Radhakrishnan, Ravi Bhargava, Lizy K. John

June 2001 **Proceedings of the 15th international conference on Supercomputing**Full text available: [pdf\(254.91 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

State of the art Java Virtual Machines with Just-In-Time (JIT) compilers make use of advanced compiler techniques, run-time profiling and adaptive compilation to improve performance. However, these techniques for alleviating performance bottlenecks are more effective in long running workloads, such as server applications. Short running Java programs, or client workloads, spend a large fraction of their execution time in compilation instead of useful execution when run using JIT compilers. In ...

**2 Special session on reconfigurable computing: The happy marriage of architecture and application in next-generation reconfigurable systems**


Ingrid Verbauwhede, Patrick Schaumont

April 2004 **Proceedings of the 1st conference on Computing frontiers**Full text available: [pdf\(398.28 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

New applications and standards are first conceived only for functional correctness and without concerns for the target architecture. The next challenge is to map them onto an architecture. Embedding such applications in a portable, low-energy context is the art of molding it onto an energy-efficient target architecture combined with an energy efficient execution. With a reconfigurable architecture, this task becomes a two-way process where the architecture adapts to the application and vice-vers ...

**Keywords:** embedded, real-time systems

**3 Energy efficiency in system design: Energy savings through compression in embedded Java environments**


G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, W. Wolf

May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**Full text available: [pdf\(621.08 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)